REMARKS

As a preliminary matter, it is noted that cited USP No. 5,815,698 to Holmann et al., which the Examiner relied on in the pending § 103 rejection, was not listed in the PTO-892 form.

Accordingly, it is AGAIN respectfully requested that the Examiner list USP No. 5,815,698 to Holmann et al. in a PTO-892 form in the next Office Action to make the record clear that it was considered by the Examiner.

Claim 7 stands rejected under 35 U.S.C. § 102 as being anticipated by Phillips et al. '743 ("Phillips"), and claims 7-8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Eickemeyer et al. '460 in view of Holmann et al. '698 ("Holmann"). Claim 7 is independent. These rejections are respectfully traversed for the following reasons.

It is respectfully submitted that none of the cited prior art, alone or in combination, disclose or suggest the claimed combination, *inter alia*, "instruction parallelizing/executing means for executing the two instructions, which designate the first execution unit as a target, in parallel by allocating one of the two instructions to the second execution unit, wherein the parallelizing/executing means is configured to convert one of the two instructions to another equivalent instruction that designates the second execution unit" as recited in claim 7. The Examiner appears to maintain the pending rejections based on interpreting the aforementioned feature of the present invention as merely a rearrangement of instructions. Accordingly, the Examiner relies on the conventional parallel processing of Phillips and Holmann as reading on the claimed invention.

However, it is respectfully submitted that the Examiner has ignored *how* the claimed instructions are rearranged. Even assuming *arguendo* the Examiner's interpretation of "convert"

Application No.: 10/621,440

is proper, notwithstanding any alleged rearrangement of instructions in Phillips and Holmann, neither discloses or suggests rearranging instructions in the particular manner recited in claim 7. Specifically, neither Holmann nor Phillips discloses or suggests a means for replacing or exchanging (as "converting" is being interpreted by the Examiner) one of the two instructions to be executed in parallel with *another <u>equivalent</u>* instruction.

As a preliminary matter, the Examiner's reliance on Phillips is not understood, as Phillips discloses only conventional parallel processing in which the 3-1 ALU is complemented with a 2-1 ALU. Phillips does not describe specifically how the instructions are arranged for execution, but only identifies the end-results. That is, the only discussion related to parallel processing appears to be at col. 9 of Phillips describing possible instructional combinations (e.g., add-add, logical-add, etc.). Indeed, on page 3, paragraph 11 (last three lines) – page 4, line 3 of the outstanding Office Action lines, the Examiner references portions of Phillips which do not exist (e.g., the Examiner references col.'s 16 and 17, ALU 63,64, etc., whereas Phillips only has 12 columns and is silent as to an ALU designated by reference numerals 63 and 64).

Nonetheless, even if the non-existent portions of Phillips which the Examiner referenced were real prior art, the Examiner's conclusions derived therefrom are not relevant to the claimed invention for reasons similar to those discussed below with respect to Holmann. That is, the Examiner's conclusion arising from Phillips is merely that a second instruction originally assigned to a first ALU is thereafter assigned to another ALU. This conclusion is completely unrelated to converting an instruction to an equivalent instruction.

Application No.: 10/621,440

Turning to Holmann, as shown in Figures 3-4, in the instance that two instructions can not be executed in parallel (i.e., SRA and SUB; col. 2, lines 55-57 of Holmann), Holmann discloses a rearrangement in which a NOP instruction is written into the slot originally slated for the SUB instruction (r4, r4, r3). Accordingly, the SUB instruction is moved from the slot located in the 2nd column, 2nd row to the slot located in the 1st column, 3rd row (*see* Figure 4 of Holmann). However, even if this modification is interpreted as a rearrangement or exchange of two instructions, such a rearrangement/exchange is NOT tantamount to an instruction being replaced/exchanged for an *equivalent* instruction so as to enable parallel execution of the originally intended instructions of SUB and SRA (i.e., <u>SUB and NOP are not equivalents</u>). Rather, in Holmann, the SRA instruction is executed in parallel with a new NOP instruction which is different from the originally intended SUB instruction.

In contrast, as shown in one exemplary form in Figures 25-26 of Applicants' drawings, instructions A (add R3, R2) and B (add R0, R0) can not be executed in parallel. Accordingly, instruction B is converted to, or replaced/exchanged with, instruction E (asl 1, RO; Figure 26) so as to enable parallel execution between instructions A and E, where instruction E is equivalent to instruction B (see Figure 5 and corresponding description thereof). In this regard, instructions B and E are equivalent similarly to how an amount of currency converted from one unit to another is equivalent (e.g., 1 dollar converted to an equivalent amount of yen, etc.). No such means for enabling equivalent instructions to be processed in parallel is disclosed in the cited prior art, and indeed, the cited prior art is not concerned with such an effect and therefore provides no motivation for achieving the claimed structure. Only Applicant has recognized and considered

such an effect, and conceived of the novel and non-obvious means which can enable realizing said effect.

Based on the foregoing, even assuming *arguendo* that the Examiner's interpretation of "convert" is accurate, it is respectfully submitted that none of the cited prior art, alone or in combination, disclose or suggest the combination as recited in claim 7.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that the cited prior art does not anticipate claim 7, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 7 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 7 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In

Application No.: 10/621,440

addition, it is respectfully submitted that the dependent claims are patentable based on their own

merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable

over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35

U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that

all claims are in condition for allowance, an indication for which is respectfully solicited. If

there are any outstanding issues that might be resolved by an interview or an Examiner's

amendment, the Examiner is requested to call Applicants' attorney at the telephone number

shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is

hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to

such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ramyar M. Farid

Registration No. 46,692

600 13th Street, N.W.

Washington, DC 20005-3096

Phone: 202.756.8000 RMF:MaM

Facsimile: 202.756.8087 Date: December 17, 2007 Please recognize our Customer No. 53080

as our correspondence address.

6